AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

[0005] The cellular phone is generally driven by a battery power supply VBAT. When an output of the battery power supply VBAT becomes lower than or equal to [[2,0]] 2.0 volts, an output of the regulator 5 also becomes lower than or equal to [[2,0]] 2.0 volts. Accordingly, a voltage detecting section is generally provided to continuously output reset signals to the CPU 2 so as to deactivate the CPU 2 in order to avoid operation when the output of the regulator 5 becomes less than or equal to a prescribed reference voltage (e.g., 1.9 volts). However, when the CPU 2 of the cellular phone enters into the power saving mode under the above-mentioned procedure, the voltage detecting section also detects such a decreased voltage and outputs a reset signal to the CPU 2. As a result, the CPU 2 is deactivated.

[0008] In another exemplary embodiment, a power supplying section switches the power supply voltage from a first to a second level that is lower than a first level, using a first switching signal. The power supplying section also changes the first switching signal from a first to a second condition when a power saving mode is set. A voltage detecting section changes the voltage detection value [[(or]] (or reset level) from a [[fist]] first to a second level, where the second level is lower than the first level, by using a second switching signal. The voltage detection section also changes the second switching signal from a first to a second condition when the power saving mode is set. The control section then changes the second switching signal from a first to a second condition after changing the first switching signal from a first to a second condition.

[0009] In yet another exemplary embodiment, the control section returns the second switching signal to the second level after returning the first switching signal to the [[fist]] first condition when the power saving mode is terminated.

[0017] Referring now to the drawings, wherein like reference numerals and marks designate identical or corresponding parts throughout several views, in particular in FIG. 1, a cellular phone 1 is described under a first exemplary embodiment. Cellular phone [[1includes]] 1 includes a power supply control section 100 that adjusts an output of a battery power supply VBAT, a CPU 2, an operational key 3,[[,]] and a reception section 4. The CPU 2 provides a power saving mode and outputs a voltage switching signal SI of a low level to the power supply control section 100 during a power saving mode. The CPU 2 also outputs a voltage switching signal SI of a high level to the power supply control section 100 during a normal operation mode.

[0019] The regulator 10 ordinarily outputs a constant voltage Vcc1 [[Vcc 1]] of 2.0 volts by transforming a battery power supply VBAT, having an initial output of 3.6 volts. The regulator 10 also outputs a constant voltage Vcc2 [[Vcc 2]] that is lower than voltage Vcc1 [[Vcc 1]] in response to a low level REG switching signal S2, which is transmitted from the control section 20. Under this configuration, the regulator 10 serves as a power supply section, supplying the CPU 2 with power in collaboration with the battery power supply VBAT.

[0021] The control section 20 decreases the prescribed voltage detection value from the first to second level in response to a low level voltage switching signal SI when a power saving mode is set (i.e., when Vcc2 is larger than the second level, and the first level is larger than the Vcc2). The first and second levels correspond to the voltage reference detection values (Vref x ((r4 + r5 + r6)/(r5 + r6))) and (Vref x ((r4 +

r5)/(r5))), respectively. Subsequently, the control section 20 decreases voltage Vcc, output from the regulator 10, down to Vcc2 from [[Vccl]] Vcc1. Further, when the low level voltage switching signal SI is stopped for the purpose of terminating the power saving mode, the control section 20 synchronously controls the regulator 10 to recover the output voltage [[Vccl]] Vcc1, and after that controls the voltage detecting section 30 to recover the first voltage level.

[0023] The regulator 10 of FIG. 2 outputs a constant voltage [[Vccl]] Vcc1 of 2.0 volts from the battery power supply VBAT, and has an initial output value of 3.6 [[3 . 6]] volts as mentioned above. The regulator 10 includes a P-channel type MOSFET 12 generating an output based upon the output from the battery power supply VBAT in accordance with a voltage applied to its gate terminal as a control signal from comparator 11. A reference voltage "Vref" generated by a regulator (not shown) is input to a positive input terminal of the comparator 11. A signal obtained by dividing an output of the MOSFET 12 with a resistance division circuit formed from resistances rl to r3 is input to a negative input terminal of the comparator 11. A switch SW1 is turned OFF by an input of [[an]] a REG switching signal S2 (a first switching signal) of a high level.

[0024] The voltage detecting section 30 includes comparator 31. A value obtained by dividing [[Vccl]] Vcc1 of 2.0 volts of the regulator 10 with a resistance division circuit formed from resistances r4 to r6. The value is then applied to a positive input terminal of the comparator 31. A reference voltage Vref generated by a regulator (not shown) is input to the negative input terminal of comparator 31. Switch SW2 is turned OFF by a high-level input of a VDET switching signal S3 (a second switching signal)

[0026] The signal generation circuit Cl includes three inverters 22, 23 and 25 [[to 24]], which are serially connected as shown in FIG. 2. A condenser 24 is disposed between the inverters 23 and 25, and is grounded at one end. The signal generation circuit C2 includes a CMOS inverter 26, driven by a constant current source 27, a condenser 28, and a buffer circuit 29.

[0030] By employing such a configuration, an erroneous output of a reset signal (e.g. ON) to the CPU 2 can be avoided. The erroneous reset signal is typically generated when either the constant voltage output Vcc descends from [[Vccl]] Vcc1 to Vcc2 (that is lower than Vrefl) before a voltage detection value defined by the voltage detection section 30 descends to the second level (i.e., v2=Vref x (r5)/(r4 +r5)) from the first level (i.e., v1 = Vref x (r4 + r5)/(r4 + r5 + r6)), or when the voltage detection value recovers the first level from the second level before the constant voltage Vcc recovers the output voltage [[Vccl]] Vcc1 from the Vcc2.

[0032] Specifically, a regulator 210 includes a P-channel type MOSFET 213 that adjusts its output in accordance with a voltage applied to its gate as a control signal in the similar manner as performed by the regulator 10 of the first embodiment. Regulator 210 includes a comparator 212 that outputs electric signals to the gate of the MOSFET 213. A reference voltage Vref provided by a regulator (not shown) is applied to a positive input terminal of the comparator 212. A D/A converter 211 is connected to a negative input terminal of a comparator 212 so as to output analog signals [[Vccl]] Vcc1 from 2.0 to 0 volts, based upon the output from the FET 213 in accordance with digital signals 0 to 256. The CPU 2 outputs [[an]] a REG setting signal (a first switching signal) of 127 values (decimal expression) to the D/A converter 211 when an operation mode runs with the ordinary voltage.